CLAIMS

1. A fast page programming architecture of a non-volatile memory electronic device, comprising:

a memory cell matrix;

an SPI serial communication interface;

circuit portions associated with the cell matrix and responsible for addressing, decoding, reading, writing and erasing of the memory cell matrix; and

a buffer memory bank for storing and outputting data during page programming in a pseudo-serial mode, wherein said buffer memory bank comprises a battery of latches storing data to be programmed and memory blocks allowing data to be latched one bit at a time and output at least two bytes at a time.

2. An architecture according to claim 1, wherein said buffer memory bank is incorporated in a state machine receiving at an input data, addresses, and instructions to enter the memory cell matrix and the state machine produces a data synchronization signal that synchronizes transfer of data in a path going from the state machine to the memory cell matrix.

3. An architecture according to claim 1, wherein said buffer memory bank also comprises two counter blocks that respectively store a first number indicating how many bytes are to be programmed and a second number indicating how many bytes have already been programmed in the matrix at each precise moment of the page programming.

4. An architecture according to claim 4, further comprising a comparator block connected downstream to said counters and susceptible of generating a reset pulse when the first number is equal to the second number of bytes .

5. An architecture according to claim 1, further comprising a control logic to take into account whether an even or odd number of bytes is to be programmed and a starting address wherein the page programming is started, as well as to provide control signals to a block responsible for loading data in program loads that load data into the memory cell matrix.

6. An architecture according to claim 1, wherein each latch includes a data input, first and second control inputs, and an output, the latch being structured to change a logic value at the output based on a logic value at the input only when triggered by respective control signals at the first and second control inputs.

7. An architecture according to claim 6 wherein each latch includes:

cross-coupled inverters positioned between first and second latch nodes, the second latch node being connected to the output;

first and second switches connected in series between the first latch node and a third latch node;

third and fourth switches connected in series between the second latch node and the third latch node, the first and third switches having respective control terminals connected together and to the first control input, and the second and fourth switches having respective control terminals connected together and to the data input; and

a fifth switch connected between the third latch node and a reference voltage and having a control terminal connected to the second control input.

8. A method for performing a page programming in non-volatile memory electronic devices equipped with a memory cell matrix and an SPI serial communication interface, as well as circuit portions associated with the cell matrix and responsible for addressing, decoding, reading, writing, and erasing of the memory cell matrix, the method comprising:

latching data in a buffer memory bank one bit at a time during the page programming through said interface; and

outputting from the buffer memory bank at least a byte of data at a time during the page programming.

9. A method according to claim 8, wherein the outputting step outputs at least two bytes at a time from said buffer memory bank.

10. A method according to claim 8, further comprising providing a Page Programming instruction that includes a Page Programming command, a memory address andall bytes from the data one after another through an input of said interface.

11. A method according to claim 8, wherein the data contained in the memory bank are overwritten when a following page programming starts without performing a reset of the bank itself.

12. A method according to claim 8, further comprising calculating how many bytes of the data are to be programmed and how many bytes are already programmed in the matrix at each precise moment of the Page Programming operation.

13. A non-volatile memory device, comprising:

a non-volatile memory cell matrix;

a data input for receiving data to be programmed into the memory cell matrix;

a buffer memory bank connected between the data input and the memory cell matrix and structured to buffer the data between the data inputand the memory cell matrix during a page programming mode, wherein the buffer memory bank comprises a battery of latches that respectively latch the data one bit at a time and output at least a byte at a time.

14. The memory device of claim 13, wherein the buffer memory bank is incorporated in a state machine receiving at an input data, addresses, and instructions to enter the memory cell matrix and the state machine produces a data synchronization signal that synchronizes transfer of data in a path going from the state machine to the memory cell matrix.

15. The memory device of claim 13, wherein the buffer memory bank also comprises two counter blocks that respectively store a first number indicating how many bytes are to be programmed and a second number indicating how many bytes have already been programmed in the matrix at each precise moment of the page programming.

16. The memory device of claim 15, further comprising a comparator block connected downstream to the counters and structured to generate a reset pulse when the first number is equal to the second number of bytes.

17. The memory device of claim 13, wherein each latch includes a data input, first and second control inputs, and an output, the latch being structured to change a logic value at the output based on a logic value at the input only when triggered by respective control signals at the first and second control inputs.

18. The memory device of claim 13 wherein each latch includes a data input, first and second control inputs, and an output, the latch being structured to change a logic value at the output based on a logic value at the input only when triggered by respective control signals at the first and second control inputs.

19. The memory device of claim 18 wherein each latch includes:

cross-coupled inverters positioned between first and second latch nodes, the second latch node being connected to the output;

first and second switches connected in series between the first latch node and a third latch node;

third and fourth switches connected in series between the second latch node and the third latch node, the first and third switches having respective control terminals connected together and to the first control input, and the second and fourth switches having respective control terminals connected together and to the data input; and

a fifth switch connected between the third latch node and a reference voltage and having a control terminal connected to the second control input.

20. The memory device of claim 19 further comprising an inverter connected between the control terminals of the second and fourth switches.

21. A memory device, comprising:

a plurality of latches each including a data input, first and second control inputs, and an output, the latch being structured to change a logic value at the output based on a logic value at the input only when triggered by respective control signals at the first and second control inputs, wherein each latch includes:

cross-coupled inverters positioned between first and second latch nodes, the second latch node being connected to the output;

first and second switches connected in series between the first latch node and a third latch node;

third and fourth switches connected in series between the second latch node and the third latch node, the first and third switches having respective control terminals connected together and to the first control input, and the second and fourth switches having respective control terminals connected together and to the data input; and

a fifth switch connected between the third latch node and a reference voltage and having a control terminal connected to the second control input.

22. The memory device of claim 21, wherein each latch further includes an inverter connected between the control terminals of the second and fourth switches.

23. The memory device of claim 21, wherein each latch further includes an inverter connected between the second latch node and the output.

24. A latch, comprising:

a data input;

first and second control inputs;

an output, the latch being structured to change a logic value at the output based on a logic value at the input only when triggered by respective control signals at the first and second control inputs;

cross-coupled inverters positioned between first and second latch nodes, the second latch node being connected to the output;

first and second switches connected in series between the first latch node and a third latch node;

third and fourth switches connected in series between the second latch node and the third latch node, the first and third switches having respective control terminals connected together and to the first control input, and the second and fourth switches having respective control terminals connected together and to the data input; and

a fifth switch connected between the third latch node and a reference voltage and having a control terminal connected to the second control input.